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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER
CIESLEWICZ, ANELA B

ART UNIT	PAPER NUMBER
[illegible]	

DATE MAILED: [illegible]

Please find below and or attached an Office communication concerning this application or proceeding.

Application No.	Applicant(s)
10/064,514	CHO, ET AL.
Examiner	**Art Unit**
Aneta B. Cieslewicz	2814

Office Action Summary

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2002*

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 8-20* is/are rejected.

7)☒ Claim(s) *4-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1.☐ Notice of References Cited (PTO-892)
2.☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3.☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 2
4.☐ Interview Summary (PTO-413) Paper No(s).
5.☐ Notice of Informal Patent Application (PTO-152)
6.☒ Other:

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because:

- they fail to show 10" and 20" as described in the specification on page 4, ¶25 and page 5, ¶26-28.

Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. **Applicant is advised to carefully review all the drawings for further needed corrections.**

Specification

2. The disclosure is objected to because of the following informalities: on page 5, ¶28 a typographical error: "amplifier 10,10" should be corrected to "amplifier 10, 10" ".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for

for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 7, 8, 10-14 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Shirakawa, EP 1 077 494 A2.

Re claim 1, Shirakawa discloses a power amplifier integrated circuit comprising: substrate (13); heat sink (12) for dissipating heat; transistor (50) disposed on the substrate, the transistor comprising a collector (3), a base (2), and at least an emitter (1); and an emitter electrode (4) directly connecting the heat sink and the emitter (i.e. Figures 1B and 16).

Re claim 2, in the power amplifier integrated circuit disclosed by Shirakawa the transistor is a heterojunction bipolar transistor (HBT) (i.e. column 10, line 25).

Re claim 3, in the power amplifier integrated circuit disclosed by Shirakawa the emitter comprises a metallization layer (metal wiring) (11).

Re claim 8, the power amplifier integrated circuit disclosed by Shirakawa comprises more than one emitter, and emitters are mutually connected by a metallization layer (i.e. column 3, lines 19-23 and Figure 6B).

Re claim 10, in the power amplifier integrated circuit disclosed by Shirakawa the heat sink is a metal layer (i.e. column 10, line 36).

Re claim 11, in the power amplifier integrated circuit disclosed by Shirakawa plurality of transistors and a plurality of emitter electrodes are disposed in an array, and operate as a functional device (i.e. column 3, lines 19-23, Figure 6B).

Re claim 12, in the power amplifier integrated circuit disclosed by Shirakawa the substrate is a GaAs substrate (i.e. column 10, line 34).

Re claim 13, Shirakawa discloses a method for manufacturing a heat dissipating power amplifier integrated circuit, the method comprising: providing a substrate (13); providing a heat sink for dissipating heat (12); forming a transistor on the substrate (57), the transistor comprising a collector (3), a base (2), and at least an emitter (1); and directly connecting the heat sink and the emitter using an emitter electrode (4) (i.e. column 11, lines 36-58, column 12, lines 1-46 and Figures 1B and 16).

Re claim 14, in the method disclosed by Shirakawa forming the transistor comprises: disposing a metallization layer (4) on the substrate to form the emitter; and disposing a second metallization layer (11) to mutually connect emitters (i.e. Figure 6B).

Re claim 16, the method of claim disclosed by Shirakawa further comprises: arraying a plurality of transistors and a plurality of emitter electrodes to form a functional device (i.e. column 3, lines 19-23 and Figure 6B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirakawa, in view of Adlerstein et al., US 5,986,324.

Re claim 9, the power amplifier integrated circuit disclosed by Shirakawa includes all the limitations claimed except that the emitter electrode and the heat sink provide an electrical ground connection to the emitter. Adlerstein et al. disclose a power amplifier integrated circuit in which the emitter electrode and the heat sink provide and electrical ground connection to the emitter (i.e. column 4, lines 24-26). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shirakawa such that the electrical ground connection to the emitter is provided through emitter electrode and the heat sink, as disclosed by Adlerstein et al., in order to form a high power HBT type device in a common emitter configuration (i.e. column 1, lines 22-28).

Re claim 15, the method disclosed by Shirakawa includes all the limitations claimed except that the emitter is electrically grounded through the emitter electrode and the heat sink. Adlerstein et al. disclose a method of manufacturing a power amplifier integrated circuit in which the emitter is electrically grounded through the emitter electrode and the heat sink (i.e. column 4, lines 24-26). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Shirakawa such that the emitter is electrically grounded through the emitter electrode and the heat sink, as disclosed by Adlerstein et al., in order to form a high power HBT type device in a common emitter configuration (i.e. column 1, lines 22-28).

5. Claims 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Sato, 5,349,239.

Re claim 17. Sato disclose a power amplifier integrated circuit comprising: a substrate (10); heat sink (4); a transistor formed on the substrate, the transistor comprising a collector (8), a base (7), and an emitter (5); and a bump (1) disposed on the emitter so as to connect the emitter with the layer for heat dissipation (heat sink) (i.e. Figure 3). Sato does not explicitly specify that the heat sink is an electrically conductive layer. However, Sato does disclose that grounding of the emitter can be affected by bonding bump electrode to the heat sink (i.e. column 5, lines 25-34). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include an electrically conductive layer in the device of Sato in order to effect grounding of the emitter.

Re claim 18, in the power amplifier integrated circuit disclosed by Sato the electrically conductive layer and the substrate sandwich the transistor (i.e. Figure 3).

Re claim 19, in the power amplifier integrated circuit disclosed by Sato the electrically conductive layer provides an electrical ground connection to the emitter (i.e. column 5, lines 25-34).

6. Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Sato, 5,349,239 in view of Shirakawa, EP 1 077 494 A2.

Re claim 20, the power amplifier integrated circuit disclosed by Sato includes all the limitations claimed except that the electrically conductive layer is a metal layer. Shirakawa discloses a power amplifier integrated circuit in which the electrically conductive layer is a metal layer (i.e. column 10, line 36). Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify

the device of Sato to include a conductive layer made of metal, as disclosed by Shirakawa, in order to provide an electrical connection to the ground.

Allowable Subject Matter

7. Claims 4, 5, 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aneta B. Cieslewicz whose telephone number is (703) 308-7607. The examiner can normally be reached M-F (8:00 a.m. - 4:30 p.m.).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached at (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.